What is claimed is:

1. A method for controlling dimensions of structures formed on a substrate using an etch process, comprising:

providing the substrate having a patterned etch mask formed thereon; measuring dimensions of elements of the mask on the substrate;

adjusting a process recipe for an etch process using the results of measuring said dimensions; and

forming the structures on the substrate performing the etch process that uses the adjusted process recipe.

- The method of claim 1 wherein the substrate is a semiconductor wafer.
- 3. The method of claim 1 wherein the mask is a patterned hard etch mask or a patterned photoresist mask.
- 4. The method of claim 1 wherein the structures are formed in at least one material layer disposed beneath the mask.
- 5. The method of claim 1 wherein the dimensions are smallest widths of the elements.
- 6. The method of claim 1 wherein the dimensions are measured using a nondestructive measuring technique.
- 7. The method of claim 6 wherein the measuring technique is an optical measuring technique.
- 8. The method of claim 1 wherein the measuring step and the forming step are performed using processing modules of a single substrate processing system.

- 9. The method of claim 1 wherein the adjusting step comprises calculating an adjustment for the process recipe of the etch process.
- 10. The method of claim 9 wherein the adjustment is an adjustment for at least one parameter related to a thickness of a film of the material removed from sidewalls of the structures during the etch process.
- 11. The method of claim 10 wherein the at least one parameter is selected from a group consisting of a duration of time for overetching the structures, a flow rate and/or pressure of an etchant gas or gases, a plasma source power, a substrate bias power, a material of the structures and a thickness of sidewalls of the structures.
- 12. A method for controlling dimensions a gate structure of a field effect transistor formed on a substrate using an etch process, comprising:

providing the substrate having a patterned etch mask formed upon a film stack of the gate structure;

measuring dimensions of elements of the mask on the substrate;

adjusting a process recipe for an etch process of etching a layer of the film stack using the results of measuring said dimensions; and

forming the structures in the layer performing the etch process that uses the adjusted process recipe.

- 13. The method of claim 12 wherein the layer is selected from a group consisting of a gate conductor layer, a gate electrode layer, and a gate dielectric layer.
- 14. The method of claim 12 wherein the gate conductor layer comprises WSi, the gate electrode layer comprises doped polysilicon and the gate dielectric layer comprises SiO₂ or HfO₂.
- 15. The method of claim 12 wherein the mask is a patterned hard etch mask or a patterned photoresist mask.
- 16. The method of claim 12 wherein the mask comprises a material selected from a group consisting of SiON, SiO₂, Si₃N₄, HfO₂ and α –carbon.

- 17. The method of claim 12 wherein the dimensions are smallest widths of the elements.
- 18. The method of claim 12 wherein the dimensions are measured using a non-destructive measuring technique.
- 19. The method of claim 18 wherein the measuring technique is an optical measuring technique.
- 20. The method of claim 12 wherein the measuring step and the forming step are performed using processing modules of a single substrate processing system.
- 21. The method of claim 12 wherein the adjusting step comprises calculating an adjustment for the process recipe of the etch process for etching the layer.
- 22. The method of claim 21 wherein the adjustment is an adjustment for at least one parameter related to a thickness of a film of the material removed from sidewalls of the layer during the etch process.
- 23. The method of claim 22 wherein the at least one parameter is selected from a group consisting of a duration of time for overetching the structures, a flow rate and/or pressure of an etchant gas or gases, a plasma source power, a substrate bias power, a material of the structures and a thickness of sidewalls of the structures.
- 24. A computer-readable medium containing software that when executed by a computer causes a semiconductor wafer processing system to control dimensions of structures formed on a substrate using an etch process, said medium using a method, comprising:

providing the substrate having a patterned etch mask formed thereon;

measuring dimensions of elements of the mask on the substrate;

adjusting a process recipe for an etch process using the results of measuring said dimensions; and

forming the structures on the substrate performing the etch process that uses

PATENT 8377/ETCH/SILICON/JB

the adjusted process recipe.

- 25. The computer-readable medium of claim 24 wherein the measuring step and the forming step are performed using processing modules of a single substrate processing system.
- 26. The computer-readable medium of claim 24 wherein the adjusting step comprises calculating an adjustment for the process recipe of the etch process.
- 27. The computer-readable medium of claim 26 wherein the adjustment is an adjustment for at least one parameter related to a thickness of a film of the material removed from sidewalls of the structures during the etch process.
- 28. The computer-readable medium of claim 27 wherein the at least one parameter is selected from a group consisting of a duration of time for overetching the structures, a flow rate and/or pressure of an etchant gas or gases, a plasma source power, a substrate bias power, a material of the structures and a thickness of sidewalls of the structures.